REMARKS

Claims 1-30 are pending in the application. Claims 1-30 stand rejected under 35 U.S.C. 112, first paragraph. Claims 1-6 and 9-29 stand rejected under 35 U.S.C. 102(b) as allegedly being anticipated by U.S. Patent No. 4,371,923 to Dinwiddie, Jr. et al. ("Dinwiddie").

Claims 7-8 and 30 stand variously rejected under 35 U.S.C. 103 as allegedly being unpatentable over Dinwiddie in view of U.S. Patent No. 5,784,699 to McMahon et al. ("McMahon"), and U.S. Patent No. 5,546,554 to Yung et al. ("Yung").

In view of the following remarks, Applicant respectfully traverses the rejections and asks that they be withdrawn. Reconsideration and allowance are respectfully requested.

I. The Rejections Under 35 U.S.C. 112

The office action alleges that claims 1-30 do not satisfy the written description requirement of 35 U.S.C. 112, first paragraph.

The Federal Circuit has made clear that the specification need not include verbatim support for claim terms. See, e.g. Purdue Pharma v. Faulding Corp., 230 F.3d 1320, 1324 (Fed. Cir. 2000). Rather, all that is needed to satisfy the written description requirement of 35 USC 112, first paragraph, is disclosure in the application that reasonably conveys to an

artisan that the inventor had possession at the time of filing of the claimed subject matter. See, e.g., In re Kaslow, 217 USPQ 1089 (Fed. Cir. 1983). The supporting disclosure need not be express but rather can be inherent. See, e.g., Atmel v. Information Storage Devices, 198 F.3d 1375, 1380 (Fed. Cir. 1999).

Here, the specification as filed includes several passages that reasonably convey to an artisan that applicants had the claimed subject matter in their possession at the time of filing.

Support for the feature that "the computer system is configured so that control accesses from the central processing unit are directed to the multi-ported memory and not to the main memory and data accesses from the central processing unit are directed to the main memory and not to the dual-ported memory" may be found, for example, on page 4, lines 3-5 of the current specification: "Computer architecture 10 offers a more efficient use of resources by directing control/status accesses to dual-ported memory 18 in controller 16, rather than to main memory 22." This portion clearly describes directing control accesses to the dual ported memory and not to ("rather than") the main memory.

Support for the feature that memory accesses are directed to the main memory and not to the dual-ported memory is found on page 8, lines 5-7, which states that "Memory controller's dual-ported memory 52 need not be restricted to reading or writing control/status accesses. In some circumstances, data may be stored in memory 52." A person skilled in the art would understand this portion to describe two situations: one in which data may be stored in memory 52 (i.e., data accesses may be directed to the multi-ported memory), and one in which the multi-ported memory is restricted to reading or writing control/status accesses (i.e., data accesses are directed to the main memory and not to the multi-ported memory). Both situations are clearly contemplated by the current specification.

Therefore, a person skilled in the art would understand that applicants had in their possession at the time of filing the claimed subject matter. Thus, claims 1-30 satisfy the written description requirement of 35 U.S.C. 112.

II. The Rejections Under 35 U.S.C. 102(b)

Claim 1

Claim 1 is patentable over Dinwiddie because Dinwiddie neither teaches nor suggests that control accesses from the central processing unit are "directed to the multi-ported memory

and not to the main memory," while data accesses from the central processing unit are "directed to the main memory and not to the multi-ported memory."

The office action asserts that column 5, lines 9-10 and 48-49 of Dinwiddie teaches that data accesses from the CPU are directed to the main memory and not to the dual-ported memory. (Please see page 3 of the office action). Since these passages discuss accesses to the dual port random access storage mechanism 22, the office action is clearly equating mechanism 22 with the main memory rather than the multi-ported memory.

Since the office action identifies mechanism 22 as the main memory of claim 1, control accesses would need to be directed to the multi-ported memory (equated with elements 25, 27, and 30 of Figure 1 in the office action), and not to mechanism 22.

However, Dinwiddie teaches that "Data passing from the channel bus 8 to the microprocessor bus 16 or vice versa is at least temporarily stored in this storage mechanism." (See column 4, lines 63-66 of Dinwiddie, where the storage mechanism refers to the dual port random access storage mechanism 22). Dinwiddie defines the term "data" in column 3, lines 47-51 as "Unless otherwise indicated by the context, the term 'Data' is used herein in its broadest sense as including any kind of

information such as alphanumeric data, status information, control information, address values, and the like."

Thus, dual port random access storage mechanism 22 performs the function of (at least temporarily) storing all data (data and control/status information) being transferred between the peripherals and the CPU. This proposition is stated even more clearly in the Abstract of Dinwiddie: "All data transfers are by way of the dual port storage unit" (referring to data transfers between a host processor and one or more I/O devices).

Other portions of Dinwiddie support the interpretation that both data and control/status information is stored in mechanism 22. For example, column 11, line 66 to column 12, line 9 of Dinwiddie teaches that for a direct program control (DPC) operation:

> ...each DPC read type command enables a 2-byte word of data or status information to be transferred from the I/O controller 2 to the host processor 1. Each DPC write type operation enables a 2-byte word of data or control information to be transferred from the host processor 1 to the I/O controller 2. The DPC data word (IDCB bits 16-31) is transferred by way of the channel data bus 34 and is stored into or transferred out of the dual port storage unit 22a, 22b, with the higher order byte (Byte 2 or bits 16-23) being stored into or read from the high byte storage unit 22a and the lower order byte (Byte 3 or bits 24-31) being stored in or read from the low byte storage unit 22b.

Thus, Dinwiddie teaches that both status and data accesses are directed to mechanism 22.

As noted in a previous reply, it appears that any modification of Dinwiddie to direct control and data accesses differently would render Dinwiddie unsatisfactory for its intended purpose. When a proposed modification would render the prior art invention being modified unsatisfactory for the intended purpose, then there is no suggestion or motivation to make the proposed modification (see MPEP 2143.01). If Dinwiddie were modified so that only data accesses (or alternately, only control/status accesses) were directed to mechanism 22, it would no longer function as a data transfer interface between the microprocessor bus and the host processor channel bus for all data. Since Dinwiddie describes this data transfer interface as "A primary feature of the new and improved I/O controller 2," (see column 4, lines 59-60 of Dinwiddie), there is no motivation to modify Dinwiddie so that control accesses are no longer directed to mechanism 22.

For at least the above reasons, claim 1 is patentable over Dinwiddie.

Claims 10, 14, 19, 23, and 27

Independent claims 10, 14, 19, 23, and 27 include features similar to those in claim 1, and are therefore patentable for at least the same reasons as stated above with respect to claim 1.

Claims 2-9, 11-13, 15-18, 20-22, 24-26, and 28-30

Claims 2-9, 11-13, 15-18, 20-22, 24-26, and 28-30 depend from the independent claims noted above, and are therefore patentable for at least the same reasons.

Claim 7

Claim 7 is patentable for at least the additional reason that there is no motivation in the references to modify Dinwiddie so that "the multi-ported memory stores reservation bits mapped to blocks of general purpose memory in the multi-ported memory."

The office action contends that although Dinwiddie does not teach this feature of claim 7, McMahon teaches reservation bits mapped to a block of general purpose memory in the multi-ported memory, and that modifying Dinwiddie to include this feature is obvious because it would provide fast search and allocation/deallocation of availability of a block. (Please see page 7 of the office action).

However, the office action equates elements 25, 27, and 30 of Figure 1 with the multi-ported memory. There is no

motivation to modify these elements to include blocks of general purpose memory and reservation bits mapped to the blocks of general purpose memory (as explained below), and so claim 7 is not obvious in view of Dinwiddie and McMahon.

Element 25 of FIG. 1 of Dinwiddie is a command register file. The function of element 25 is described, e.g., in column 5, lines 28-35 of Dinwiddie:

> Each of th I/O units 306 is assigned its own unique device address. An address decoder 23 monitors the channel bus 8. When it detects the occurrence of the unique device address for one of the I/O units 3-6, it generates an address gate capture signal on its output line 24. This signal is supplied to a four-byte command register file 25 to cause the storage therein of the one-byte I/O command then appearing on the channel bus 8.

That is, element 25 is a 4-byte register file for storing I/O commands. There is no teaching or suggestion that element 25 includes blocks of general purpose memory, or reservation bits mapped to the blocks of general purpose memory, as recited in claim 7. Element 25 would need to be significantly modified to include these features. Further, there is no motivation in the references for doing so.

The asserted motivation—for providing fast search and allocation/deallocation of availability of a block—is not applicable to a 4-byte register file for storing I/O commands, such as element 25.

Element 27 of FIG. 1 of Dinwiddie is a cycle steal address register. According to Dinwiddie:

> The cycle steal address register 27 is a 16-bit register and, for example, may be comprised of a pair of Intel 8282 8-bit input/output port units. The main storage address to be sent to the host processor 1 is obtained from the DMA controller 13 via microprocessor address buses 38a and 38b and is strobed into the address register 27 by the output signal from an AND circuit 58.

Like element 25, element 27 would need to be significantly modified to include both blocks of general purpose memory and reservation bits mapped to the blocks of general purpose memory. The asserted motivation is inapplicable to element 27, since there is no need to search an address register such as element 27 to allocate/deallocate blocks.

Element 30 of FIG. 1 of Dinwiddie is a handshake, interrupt and miscellaneous controls unit. According to Dinwiddie, the function of element 30 is as follows:

> Operation of the DMA controller 13 is controlled by host DMA request logic 28. For any given multiword cycle steal transfer operation, the address counters and the word counter in the DMA controller 13 are initially loaded to the proper starting values by the microprocessor 11. Then the microprocessor 11 issues appropriate "start" signals to the request logic 28 via lines 29. Thereafter, the DMA controller 13 and the request logic 28 take over to handle the cycle stealing of the multi-word block of data. For each word transfer, the request logic 28 sends to a handshake, interrupt and miscellaneous controls unit 30 a cycle steal request signal via line 31. In response thereto, the controls unit 30 sends a

cycle steal request signal to the host processor 1.

That is, element 30 receives a cycle steal request signal and sends a cycle steal request signal to the host processor. There is no teaching or suggestion that element 30 includes blocks of general purpose memory, and so there is no motivation to modify element 30 to include reservation bits mapped to the blocks of general purpose memory. Again, since element 30 does not include blocks of general purpose memory, the asserted motivation is inapplicable.

For at least these additional reasons, claim 7 is patentable over Dinwiddie and McMahon, alone or in combination. Applicant believes that claims 1-30 are in condition for allowance and asks that all claims be allowed. No fee is believed to be due at this time. Please apply any other charges or credits to Deposit Account No. 06-1050.

Respectfully submitted,

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